REMARKS

Claims 2-13 and 15-20 remain pending in the present application. Claims 1 and 14 have been canceled. Claims 2, 7, 8, 15, 16, and 19 have been amended.

Embodiment of the Present Invention

To aid the Examiner's understanding of the present invention, an embodiment of the present invention will be briefly described.

In an embodiment of the present invention as disclosed, *inter alia*, on page 3 of the specification, the sense amplifier, once operational, generates an output voltage indicating the state of the fuse being sensed. However, the time for the sense amplifier to complete the sensing operation and settle upon an output voltage value varies depending upon numerous factors. Furthermore, because one of the output voltage states of the sense amplifier is the same as the output voltage of the sense amplifier in the powered down state, the point when the sense amplifier has settled on an output voltage can not necessarily be detected from the output voltage of the sense amplifier. However, the validation circuit tracks or mimics the operation of the sense amplifier, but is structured such that the output voltage produced thereby transitions as the sense amplifier is settling on an output voltage, regardless of the a state of the fuse. As such, the validation circuit detects and indicates when the sense amplifier has sufficiently settled on an output voltage indicating the state of the fuse.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 8-13 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant respectively traverses.

The Examiner asserts that it is not clear how the validation circuit 70 dynamically adjusts a validation point based on sense amplifier operating conditions where the output of the sense amplifier 50 is not coupled to the validation circuit 70. Applicant asserts that the output of the sense amplifier 50 is not being adjusted by the validation circuit 70 and that it is not necessary that the validation circuit 70 be connected to the output of the sense amplifier 50.

The Examiner additionally asserts that the validation circuit 70 has no relationship with the sense amplifier. Applicant respectfully disagrees. As shown in FIG. 1A, the validation circuit 70 does have a relationship with the sense amplifier 50. The validation circuit 70 and the sense amplifier 50 are made up of similar components; the validation circuit 70 having weaker transistors 72, 74, than the sense amplifier transistors 54, 56. Moreover, the gate of the sense amplifier transistor 54 and the gate of the validation circuit transistor 72 share the same input. Additionally, the gate of the sense amplifier transistor 56 and the gate of the validation circuit 74, also share the same input. FIG. 1A clearly discloses that there is a relationship between the sense amplifier 50 and the validation circuit 70.

Moreover, as shown in FIGs. 2G, the validation circuit output INVALID also reflects the dynamic operation of the validation circuit 70 and a dynamically adjusted validation point. Given that the validation circuit 70 has similar components as the sense

amplifier 50 and the gates of the validation circuit 70 and sense amplifier 50 share the same inputs as discussed above, it is clear that the validation circuit dynamically adjusts the validation point based on sense amplifier operating conditions.

Applicant asserts that claims 8-13 are clearly recited and respectfully request the grounds of rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1-5, 7-11, 13-16, and 18-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Aoki (U.S. Patent No. 6,125,069). Applicant respectfully traverses.

With regard to claims 1, 8, and 14, Applicant asserts that the rejection is now moot given the cancellation of claims 1 and 14 and the amendment of claim 8.

With regard to claim 18, Applicant asserts that Aoki fails to disclose a validation circuit mimicking, with a delay, the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid as recited in claim 18. Instead, Aoki discloses in FIGs. 3 and 15 an enable fuse 42 that is cut based on whether or not a memory cell is to be replaced by a redundant memory cell. A fuse section 22 is also shown that includes a fuse 10. The fuse section 22 is connected to a latch section 24 that latches fuse state data based on a threshold and a voltage drop across the fuse. The fuse 10 state data indicates whether or not the fuse 10 is cut.

In the rejection of claim 18, the Examiner suggests that the enable fuse 42 is a buried fuse and that elements (transistors 32 and 28) of fuse determination circuit 44_0 make up a sense amplifier. Further, the Examiner suggests that elements (transistors 28, 32 and inverters 17, 18) of fuse determination circuit 44_8 and fuse 10_8 make up a

validation circuit. Applicant respectfully disagrees with the Examiner's mapping of Aoki to claim 18.

Aoki discloses in FIG. 3 and the discussion thereof, that the fuse determination circuit 44_0 is used to determine the state of the enable fuse 42, while the fuse determination circuit 44_8 is used to determine the state of fuse 10_8. Aoki does not disclose (as alleged by the Examiner) that the fuse determination circuit 44_8 and fuse 10_8 are used to indicate when the output of the determination circuit 44_0 (the Examiner's alleged sense amplifier) are valid as suggested by the Examiner. Accordingly, Aoki does not disclose a validation circuit indicating when a sense amplifier output is valid. Therefore, Aoki cannot disclose or suggest a validation circuit mimicking, with a delay, the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid as recited in claim 18. Aoki does not disclose each and every element of independent claim 18.

With regard to dependent claims 2-5, 7-11, 13, 15, 16, and 19-20 Applicant asserts that they are allowable at least because they depend from independent claim 18 which is allowable.

Applicant respectfully requests that the art grounds of rejection be withdrawn.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 6 and 17 are allowable. Applicant has not put claim 6 into independent form at this time because claim 6 depends from independent claim 18, which is allowable.

CONCLUSION

In view of the foregoing, Applicant submits that claims 2-13 and 15-20 are patentable, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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